REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated November 19, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-15 are under consideration in this application. Claims 1 and 5 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention.

Additional Amendments

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-15 were rejected under 35 U.S.C. § 103(a) as being unpatenable over US Pat. No. 5,091,784 to Someya et al. (hereinafter "Someya")in view of US Pat. No. 6,144,355 to Murata et al. (hereinafter "Murata"), and further in view of US Pat. No. 6,211,849 to Sasaki et al. (hereinafter "Sasaki"). This rejection has been carefully considered, but is most respectfully traversed.

The liquid crystal display device of the invention (Embodiment 1 in Fig. 2 and Embodiment 2 in Fig. 23), as now recited in claim 1, includes a liquid crystal display panel 100, a plurality of cascade-connected liquid crystal drive circuits 130, 140 (Fig. 1) for sequentially transferring a signal (Fig. 1; page 1, third line to the bottom; "*the display data and clock signal as sent out of the timing controller will be delivered and passed between respective drain drivers in a one-by-one manner*" page 3, lines 17-19), and a plurality of signal lines (Fig. 1, not numbered) formed over an edge portion of the liquid crystal display panel for transmitting a

signal between any two of the drive circuits. Each of the drive circuits comprises: an image input terminal connected with one of the signal lines to receive an image signal being input thereto; a clock input terminal connected with another one of the signal lines to receive an external clock signal being input thereto; a clock compensation circuit 200 (e.g., a phase-locked loop in Fig. 3, page 17, 2nd and 3rd paragraph) for generating an internal clock signal CLL2 based on the external clock signal CL2i thereby compensating for a duty ratio deviation of the external clock signal CL2i (page 3, last paragraph; page 4, lines 20-23; page 6, line 9; page 15, 4th paragraph; page 50, 4th paragraph), said internal clock signal CLL2 swinging from a first voltage to a second voltage lower than the first voltage; a data storage circuit CST for storing therein the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal CLL2 (Fig. 12; page 24, line 18 to page 25, line 5); a data bus for transmitting the image signal from the data storage circuit; a voltage select circuit for selecting from the image signal on the data bus a voltage used to drive the liquid crystal display panel and then outputting the voltage selected; and a clock signal output circuit 134 ("BB" side of Fig. 10; p. 23, 4th & 5th paragraphs) for outputting the internal clock signal (i.e., the compensated external clock data) as a subsequent external clock signal CL2o ("*A display data latch clock signal as will be output to the outside [a subsequent cascade-connected drain driver] from the drain driver 130 is indicated by CL2o.*" page 15, 3rd paragraph; Fig. 2) to a subsequent liquid crystal drive circuit. In particular, the clock signal output circuit 134 having a delay circuit 51 (Fig. 10; p. 24, line 3; p. 35, line 12- p. 36, line 6) which delays the internal clock signal to become the subsequent external clock signal CL2o to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme.

As the clock signal duty ratio variation increases via the increase of drive circuit stages, it will finally become impossible to accept any display data at the later driver circuits. The present invention avoid the problem by compensating the duty ratio of each external clock signal form one drive circuit to a subsequent drive circuit via a delay circuit 51 for delaying the internal clock.

As shown in FIG. 17, in a dual-edge accept scheme (also see Fig. 32, p. 2, last line to p. 3, line 8) applied by the invention for taking or "accepting" display data at both the rise-up time point and drop-down point of a clock signal, marginal spaces or "clearances" are required in the setup period and the hold period such that the clock signal CLL2's riseup point and

dropdown point be each placed at an *intermediate* point between time points whereat display data changes (p. 35, 3rd full paragraph). However, the data storage circuit CST stores an image signal at a timing of a voltage changing from a first voltage to a second voltage or at a timing of a voltage changing from a second voltage to a first voltage of the internal clock signal in dual edge accept/import scheme). In the timing chart FIG. 12, the changeover points of display data as sent from the multiplex circuit 41 ("BB" side of Fig. 10; p. 33, line) are *identical to* (rather than at an *intermediate* point therebetween) the riseup point and dropdown point of the clock signal CLL2 (p. 35, last paragraph). This makes it impossible for a drain driver 130 at the next stage to take any display data into its flip-flop circuits 1-3 ("AA" side of Fig. 10) in the dual-edge accept scheme. As such, the delay circuit 51 is provided to ***delay*** of the timing/phase (p. 36, line 4) of the internal clock signal synchronized with the timing of the image signals to become the external clock signal to the subsequent liquid crystal drive circuit with the necessary marginal spaces or "clearances" for the subsequent drive circuit.

The invention (Embodiment 3 in Figs. 24-25), as now recited in claim 5, is also directed to a liquid crystal display device having a liquid crystal display element 52, a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display element for transmitting a signal between any two of the drive circuits. Each of the liquid crystal drive circuits comprises: a data input terminal connected with one of the signal lines to receive an image signal being input thereto; a clock compensation circuit for inputting an external clock signal and outputting an internal clock signal, the internal clock signal having a first period for outputting a first voltage and a second period for outputting a second voltage; a data latch circuit for taking thereto the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal; a data bus for transmitting the image signal from the data latch circuit; a voltage output circuit for outputting a voltage selected from the image signal on the data bus to the liquid crystal display element; a data output circuit for outputting the image signal on the data bus to a subsequent liquid crystal drive circuit; a clock circuit being operable to correct a duty ratio deviation of the external clock signal to provide the internal clock signal; and a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal to a subsequent liquid crystal drive circuit. In particular, the clock signal output circuit having a delay circuit, and the internal clock signal is delayed to become the subsequent external clock signal by the delay circuit so as to

provide phase margins thereof in a dual-edge accept scheme.

Applicants respectfully contend that neither Someya nor any other cited prior art reference teaches or suggests such "a delay circuit for delaying the internal clock signal to become the subsequent external clock signal CL2o to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme" as the invention.

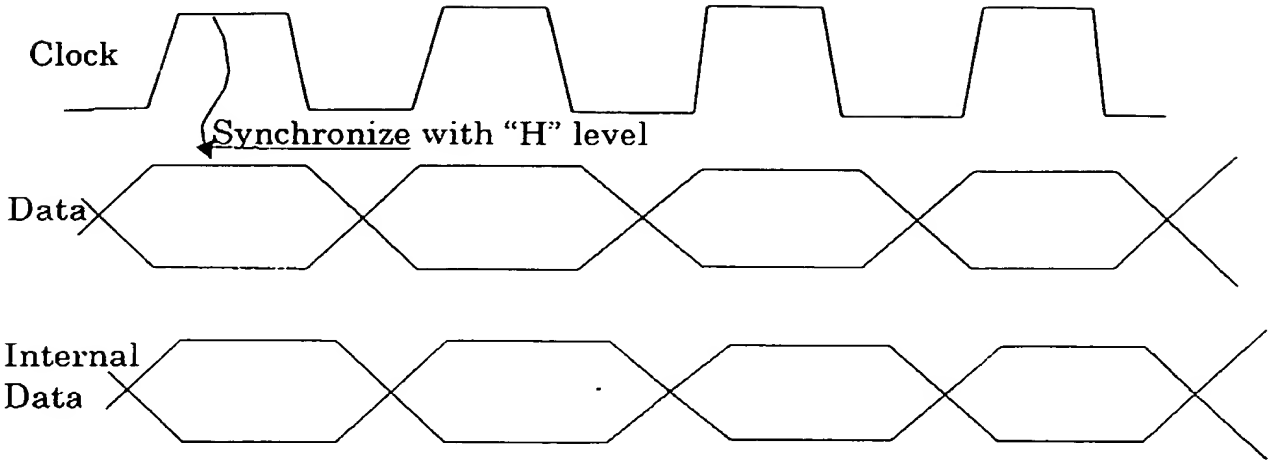
As admitted by the Examiner (p. 3, last paragraph of the outstanding Office Action), Someya and Murata do not disclose a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal to a subsequent liquid crystal drive circuit. Accordingly, Someya and Murata also fail to disclose any such a clock signal output circuit having a delay circuit to assist clock signal output circuit to perform its function by delaying the internal clock signal to become the subsequent external clock signal CL2o to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme.

The clock signal output circuit in Figs. 4-5 of Sasaki is relied upon by the Examiner to teach the clock signal output circuit 134 of the invention. However, Sasaki's duty cycle regulator 6 only "***shapes the waveform*** *of the clock signal* (col. 5, lines 10-12, lines 20-21)," rather than ***delays the timing/phase*** of the clock signal. For example, the duty cycle regulator 6 shapes the waveform of the clock signal by adjusting the threshold voltage value thereof to trace the average value of the clock signal voltage (col. 5, lines 26-27), rather than timing. Further, Sasaki does not relate to providing any phase margins between the clock signals and the display signals in a dual-edge accept scheme.

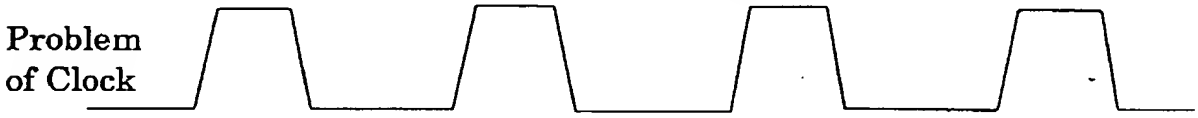
Sasaki applies only a general (synchronism) scheme (see attached drawings), rather than the dual-edge accept scheme applied by the invention. In particular, Sasaki's display control circuit performs "*an operation of sequentially supplying the pixel data signal to the signal lines in synchronism with the clock signal under the control of the control signal* (col. 4, lines 14-17)". "*The pulse width of a clock signal is decreased by 40 ns at worst each time the clock signal passes one driver IC. Therefore, in order to ensure a normal signal transmission, the number of driver ICs connected in cascade must be limited to about 10 at most*(col. 2, limes 19-23)."

In other words, Sasaki actually teaches away from the dual-edge accept scheme applied by the invention by latching the pixel data signal and the control signals to synchronize with (rather than "delay") the timing of the clock signal ("*a second latch circuit 7 for simultaneously latching the pixel data signal and the control signal output from the first latch circuit 5, in response to the clock signal output from the duty cycle regulator 6*" col. 4, lines 63-67) so as to

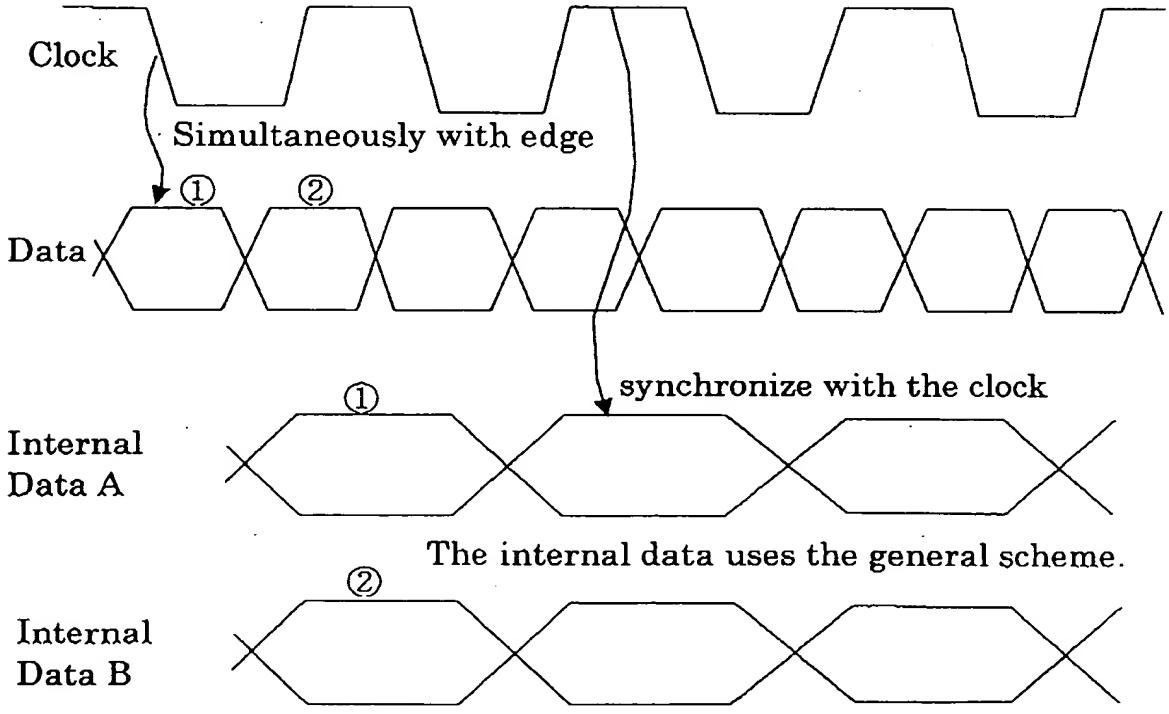
Sasaki (General scheme)



Pulse width is decreased (decrease data "H" level)



Dual edge accept scheme



recover the waveform shapes of the signals distorted during transmission with the latch circuits 5 and 7 ("*The waveforms of the pixel data signal and the control signals are shaped by the latch circuits 5 and 7*" col. 5, lines 18-19, 21-24). It is well established that a rejection based on cited references having principles that teach away from the invention is improper.

Applicants contend that neither Someya nor Murata or Sasaki teaches or discloses each and every feature of the present invention as disclosed in at least independent claims 1 and 5. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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